Monolithic Transformers for Silicon RF IC Design

John R. Long, *Member, IEEE*

***Abstract*—A comprehensive review of the electrical performance of passive transformers fabricated in silicon IC technology is presented. Two types of transformer construction are considered in detail, and the characteristics of two-port (1 : 1 and 1 : n turns ratio) and multiport transformers (i.e., baluns) are presented from both computer simulation and experimental measurements. The effects of parasitics and imperfect coupling between transformer windings are outlined from the circuit point of view. Resonant tuning is shown to reduce the losses between input and output at the expense of operating bandwidth. A procedure for estimating the size of a monolithic transformer to meet a given specification is outlined, and circuit examples are used to illustrate the applications of the monolithic transformer in RF ICs.**

***Index Terms*—Baluns, monolithic transformers and inductors, radio frequency integrated circuit design, silicon technology, transformer circuit models, wireless circuits.**

I. Introduction

TRANSFORMERS have been used in radio frequency (RF) circuits since the early days of telegraphy. Recent work has shown that it is possible to integrate passive transformers in silicon IC technologies that have useful performance characteristics in the 1–3-GHz frequency range, opening up the possibility for IC implementations of narrowband radio circuits [1], [2]. However, the limitations of RF IC transformers on silicon must be clearly understood by the circuit designer in order to make intelligent design compromises. In this paper, the construction and performance characteristics of monolithic transformers fabricated in production silicon VLSI technologies will be presented from both measurement and simulation. Although these devices are distributed parameter structures, many of the limitations inherent in their implementation on an IC chip can be examined from the circuit point of view using a lumped equivalent circuit model. In addition, the use of resonant tuning to reduce the substantial losses that arise from imperfect magnetic coupling between the windings of a monolithic transformer is described. Finally, a simplified procedure to estimate the dimensions of a transformer to meet a desired electrical specification is outlined, and examples of monolithic transformers in RF circuit applications are described. While this paper addresses transformers fabricated in silicon IC technologies, it should be noted that the results of this study are more generally applicable to components fabricated on insulating and semi-insulating substrates, such as GaAs.

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The author is with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada.

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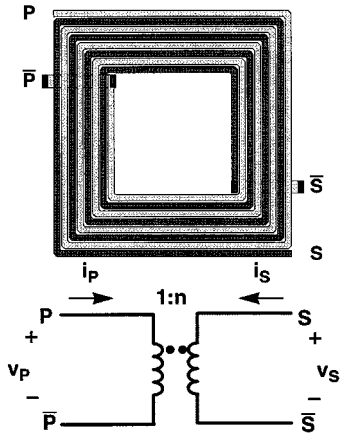

Fig. 1. Monolithic transformer. (a) Physical layout. (b) Schematic symbol.

II. Monolithic Transformer

The operation of a passive transformer is based upon the mutual inductance between two or more conductors, or windings. The transformer is designed to couple alternating current from one winding to the other without a significant loss of power, and impedance levels between the windings are transformed in the process (i.e., the ratio of terminal voltage to current flow changes between windings). In addition, direct current flow is blocked by the transformer, allowing the windings to be biased at different potentials.

To realize a lumped inductance, microwave designers often use an electrically short transmission line (i.e., guided wavelength, $\lambda_g \ll$ physical length) [1]. The input impedance of such a transmission line when short-circuited at one end is given by

$$Z_{\text{in}} \approx r + j\omega l \tag{1}$$

where r is the series resistance and l is the series inductance of the transmission line segment. The inductance is increased by making the characteristic impedance Z_0 of the line larger, however, due to r losses also increase.

A microstrip line is the simplest on-chip element for monolithic implementation of a transmission line inductor, and the strip is normally wound into a spiral to reduce chip area of the component. Interwinding microstrip spiral inductors to magnetically couple independent conductors is a logical extension of this concept, and results in a monolithic transformer, as shown in Fig. 1.

An early example of this type of structure is the compact spiral directional coupler reported by Shibata in 1981 [3]. This was followed by a circuit demonstration of a monolithic transformer in a push–pull amplifier, and later, transmitter and image-reject mixer circuits fabricated in gallium-arsenide (GaAs) IC technology by Podell [4], [5]. The first analysis of monolithic transformers was published by Frlan [6], who

compared simulation and experimental measurement for a monolithic spiral transformer and a transformer balun. Boulouard and Le Rouzic [7] proposed an alternate topology and analysis technique for monolithic microwave integrated circuit (MMIC) spiral transformers, which was also verified experimentally. Frlan and Rabjohn [8] demonstrated square spiral transformers on alumina and GaAs substrates, and developed circuit simulation tools based upon extraction of a lumped element model for the transformer from physical and geometric parameters. This modeling technique was later extended to the analysis of planar structures on conductive substrates, such as silicon [1], [9]. In the recent literature, there are many examples of monolithic transformers fabricated in silicon IC technology for use in RF circuits, such as preamplifiers [10], [11], oscillators [12], [13], mixers [2], [14], [15], and power amplifiers [16]. However, there is little design information or analysis of different transformer topologies given in the majority of these publications, which is the objective of this paper.

III. Electrical Characteristics and Construction

A planar monolithic transformer constructed from interwound metal conductors is shown in Fig. 1. Magnetic flux produced by current i_P flowing into the primary winding at terminal P induces a current in the secondary winding that flows out of terminal S. This produces a positive voltage v_S across a load connected between terminals S and $\overline{S}$. The main electrical parameters of interest to a circuit designer are the transformer turns ratio n and the coefficient of magnetic coupling k_m. The current and voltage transformations between windings in an ideal transformer are related to the turns ratio by the following equation:

$$n = \frac{v_S}{v_P} = \frac{i_P}{i_S} = \sqrt{\frac{L_S}{L_P}} \tag{2}$$

where the primary and secondary voltages (v_P, v_S) and currents (i_P, i_S) are defined in Fig. 1(b), and L_P, L_S are the self-inductances of the primary and secondary windings, respectively. The strength of the magnetic coupling between windings is indicated by the k-factor, as

$$k_m = \frac{M}{\sqrt{L_P L_S}} \tag{3}$$

where M is the mutual inductance between the primary and secondary windings. The self-inductance of a given winding is the inductance measured at the transformer terminals with all other windings open-circuited. If the magnetic coupling between windings is perfect (i.e., no leakage of the magnetic flux), k_m is unity, while uncoupled coils have a k-factor of zero. A practical transformer will have a k-factor somewhere between these two extremes. Since the materials used in the fabrication of an IC chip have magnetic properties similar to air, there is poor confinement of the magnetic flux in a monolithic transformer and $M < \sqrt{L_P L_S}$. Thus, the k-factor is always substantially less than one for a monolithic transformer, however, coupling coefficients as high as 0.9 are realizable on-chip.

The phase of the voltage induced at the secondary of the transformer depends upon the choice of the reference terminal. For an ac signal source with the output and ground applied between terminals P and $\overline{P}$, there is minimal phase shift of the signal at the secondary if the load is connected to terminal S (with $\overline{S}$ grounded). This is the noninverting connection. In the inverting connection, terminal S is grounded and $\overline{S}$ is connected to the load so that the secondary output is antiphase to the signal applied to the primary. Aside from the phase shift between input and output ports, other aspects of the transformer's electrical behavior depend upon the choice of terminal configuration (this is addressed in Section V).

A. Physical Layout

A monolithic transformer is constructed using conductors interwound in the same plane or overlaid as stacked metal, as shown in Fig. 2. The mutual inductance (and capacitance) of the transformer is proportional to the peripheral length of each winding. Interleaving planar metal traces or overlaying (i.e., stacking) conductors maximizes the periphery between windings and promotes mutual inductance at the expense of increased interwinding capacitance. The magnetic coupling coefficient k_m is determined by the mutual and self-inductances, which depend primarily upon the width and spacing of the metal traces and the substrate thickness [17], with $0.75 \leq k_m \leq 0.9$ for transformers fabricated using parameters typical for silicon VLSI technologies.

Many of the techniques that have been applied to optimization of monolithic spiral inductors are also applicable to the transformer [18], [19]. For example, ohmic losses are reduced when multiple layers of metal (available in a VLSI technology) are used to construct each winding. Although uniform width and spacing of the metal traces is typically used, nonuniform width and spacing may offer some performance advantages in specific applications [20].

The Shibata coupler [3] of Fig. 2(a) is constructed from two parallel conductors that are interwound to promote edge coupling of the magnetic field between windings. The primary and secondary terminals (labeled P and S in the figure) lie in the same plane, as illustrated in the cross-section at the right of the figure. The conductors used to connect the inner terminals to other circuitry are not shown for clarity. The square layout is defined by the outer and inner conductor lengths (OD and ID in Fig. 2), the number of turns of metal on each winding N_t ($N_t = 3$ for all designs shown in Fig. 2), and by the width w and spacing s between the metal traces. One disadvantage of Shibata's design is that the total (i.e., unwound) length of primary and secondary windings (and hence the self-inductances L_P and L_S) are not equal because the windings are asymmetric. Therefore, the transformer turns ratio $n \neq 1$ [from (2)] although there are the same number of turns of metal on each winding.

This inherent asymmetry is eliminated through the use of identical interwound spirals, as in the Frlan-style transformer [6] shown in Fig. 2(b). This ensures that electrical characteristics of primary and secondary are identical when they have the same number of turns. Another advantage of this design is that the transformer terminals are on opposite sides of the physical layout, which facilitates connections to other circuitry.

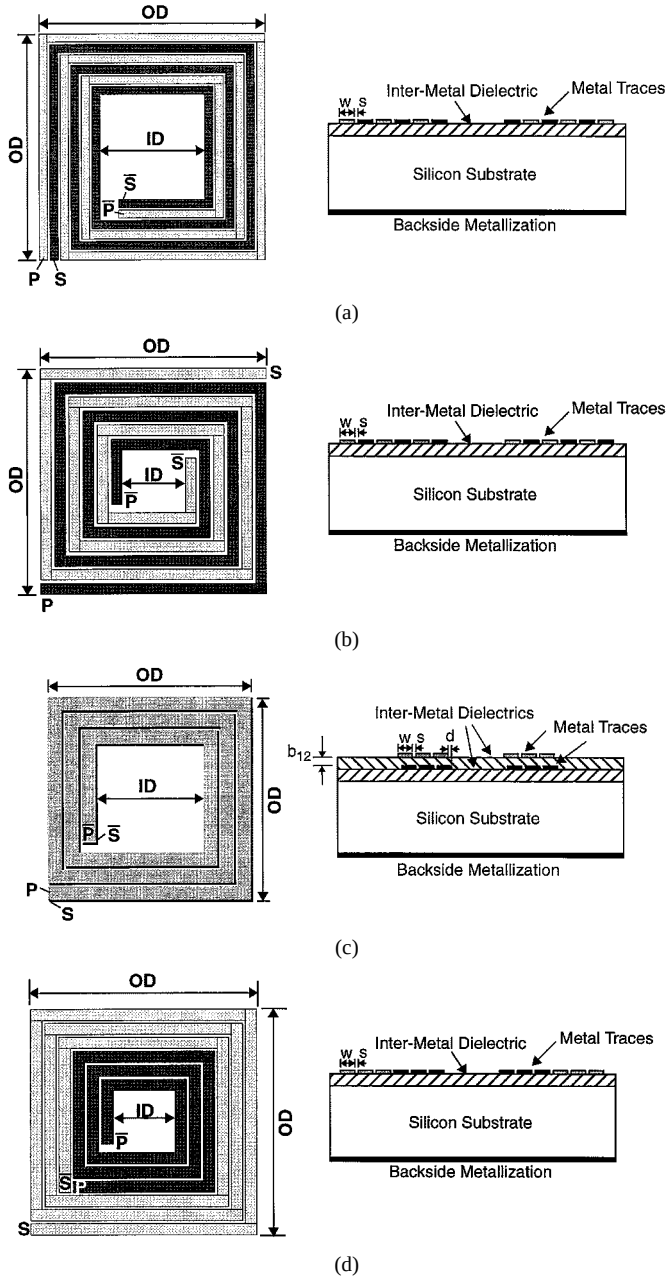

Fig. 2. Monolithic transformer winding configurations. (a) Parallel conductor (Shibata) winding. (b) Interwound (Frlan) winding. (c) Overlay (Finlay) winding. (d) Concentric spiral winding.

Multiple conductor layers (i.e., stacked conductors) are used to fabricate an overlay or broadside coupled transformer, as illustrated in Fig. 2(c). This implementation was first described by Finlay for spiral inductors [21], [22]. The Finlay-type winding utilizes both edge and broadside magnetic coupling to reduce the overall area required in the physical layout. Flux linkages between the conductor layers is improved as the intermetal dielectric is thinned [i.e., decreasing b_{12} in Fig. 2(c)]. Typically, the dielectric thickness between layers is on the order of 1 μm when fabricated on an RF IC, giving k_m close to 0.9. Although the windings as shown in the figure are identical, they are implemented on different metal layers causing asymmetry in the electrical response of the transformer. Part of this asymmetry arises from the difference in thickness between metal layers in most VLSI interconnect schemes, which results in unequal resistances for the upper (shaded) and lower (solid black) windings. Also, the upper winding is electrically shielded from the conductive substrate by the lower winding, and hence the parasitic capacitance to the conductive substrate (and the associated dissipation) differ for each winding. In addition, there is a large parallel-plate component to the capacitance between windings due to the overlapping of metal layers, which limits the frequency response. However, this can be reduced by offsetting the upper and lower metal layers by some distance d as shown in the cross-section of Fig. 2(c). These performance impairments are balanced by a savings in chip area when the windings are stacked vertically. It is expected that the current trend in silicon technologies toward thicker and lower permittivity intermetal dielectrics and more layers of interconnect metal will result in improved performance from stacked winding transformers in future.

A transformer can also be implemented using concentrically wound planar spirals as illustrated in Fig. 2(d) [23]. The common periphery between the two windings is limited to just a single turn. Therefore, mutual coupling between adjacent conductors contributes mainly to the self-inductance of each winding and not to mutual inductance between the windings. As a result, the concentric spiral transformer has less mutual inductance and more self-inductance than the Frlan and Finlay configurations, giving it a lower k-factor. However, coupling coefficients as high as 0.6 have been reported [16]. Also, there is no symmetry between windings in this configuration. Since higher k-factors (i.e., closer to the ideal k-factor of unity) are available from other configurations, the applications for this type of transformer are limited. However, a low ratio of mutual inductance to self-inductance is useful in applications such as peaking coils for high-performance broadband amplifiers [24].

IV. Electrical Models

An electrical model of a transformer that can be derived from the physical layout and process technology specifications is required for the simulation and optimization of RF circuits. The complete electrical behavior of monolithic transformers cannot be accurately predicted from closed-form equations, and hence numerical methods must be used. The numerical solution of Maxwell's equations in three dimensions will give the most accurate results, and this technique is becoming more practical for the design of multiturn spiral transformers as computing technology and simulation software improve. However, at the present time, the processing time and memory requirements for full 3-D simulation of all but the simplest transformer physical layouts are prohibitive, making this an inefficient alternative for design and optimization.

A. Multisection Lumped-Element Models

A model for the silicon RF IC transformer based on a lumped-element equivalent circuit is an efficient and accurate alternative to other numerical methods. The lumped-element approximation is valid because the physical length of each conducting segment is typically much less than the guided wavelength, λ_g in-band (i.e., OD $\ll$ λ_g). In this work, the

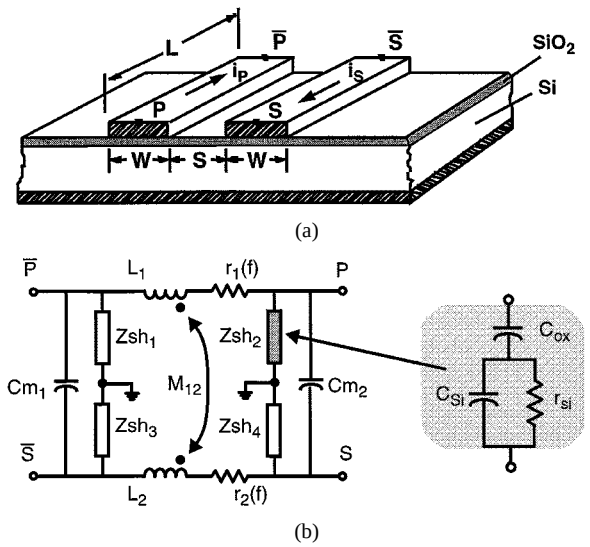

Fig. 3. Monolithic transformer compact model. (a) Cross-section of a simple two-conductor transformer. (b) Lumped-element model for a two-conductor transformer.

lumped-element circuit model is extracted from the physical layout and process technology specifications using the GEMCAP2 computer program [8], [9]. Similar models have been developed by others [25], [11]. The GEMCAP2 transformer model consists of cascaded lumped-element sections, which captures the distributed parameter behavior of an ensemble of individual conductor segments. As an example, the equivalent circuit model for the coupled microstrip transmission lines shown in Fig. 3(a) is illustrated in Fig. 3(b). Self-inductance and (frequency-dependent) ohmic losses of the conductors are modeled by components L and $r(f)$, while the parasitic capacitances and dissipation in the substrate are represented by shunt elements C_{ox}, C_{si}, and r_{si}. Transformer action is modeled by including mutual magnetic M and electric C_m coupling between the individual conducting segments. This circuit model can be used directly in a time-domain (i.e., SPICE) or frequency-domain circuit simulation. For multiturn monolithic transformers, the simple two-conductor model is extended by extracting similar lumped-element equivalent circuits for each conducting segment in the physical layout.

For transformers fabricated on silicon, losses cause by dissipation of the electric field in the substrate is accurately modeled by resistor r_{Si} for substrate resistivities greater than approximately 1 Ω·cm. Hasegawa [26] has shown that longitudinal currents in the substrate are induced by current flow along each conducting strip, and losses associated with this current are proportional to the square of frequency. Also, the current distribution across each conducting strip is frequency dependent due to the proximity and skin effects, and introduce additional losses that increase proportionally to the square root of frequency. These losses are modeled by adding frequency-dependent components to the series resistance $r(f)$ in the equivalent circuit.

B. Compact Models

The lumped-element model generated by GEMCAP2 has hundreds of circuit elements (i.e., L, C, and R) for a typical monolithic transformer with three to four turns on each winding. For design optimization, component library generation, and hand analysis purposes, a simplified version of the lumped-element model, or a compact model, is required.

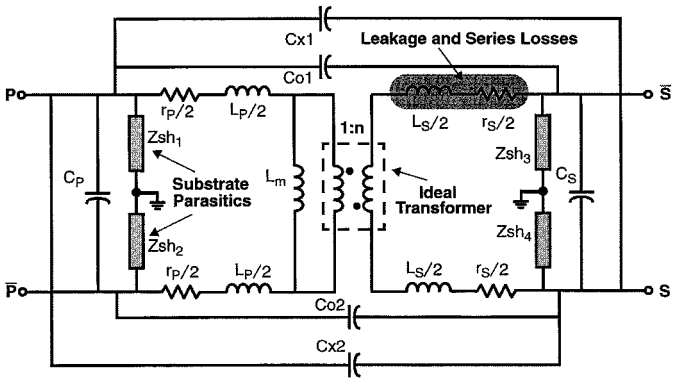

Fig. 4. $1:n$ transformer compact model.

An example of a compact model for a transformer with four independently driven ports (i.e., P, $\overline{P}$, S, and $\overline{S}$) and turns ratio $1:n$ is shown in Fig. 4. In many applications, the compact model can be further simplified because one (or more) of the ports is grounded. At the core of the model is an ideal linear transformer with magnetizing inductance L_m and turns ratio $1:n$. The path for magnetic flux between windings has the same permeability as free space for conventional IC technologies (unless, for example, a ferromagnetic layer is used in fabrication) and therefore the magnetizing inductance is lossless and the magnetic path is highly linear. Note that this is an advantage in RF IC applications, where the dynamic range (and hence linearity) requirements are very demanding. Inductances L_P and L_S are placed in series with the primary and secondary windings of the linear transformer to account for imperfect coupling or leakage of the magnetic flux between the windings. Resistors r_P and r_S are placed in series with the leakage inductances represent ohmic losses in the windings, which are significant due to the relatively thin layers of metal available in an IC process. The interwinding capacitance is modeled by capacitors connected between primary and secondary, C_o and C_x. The dominant capacitive parasitics between each winding and the underlying substrate (Z_{sh}) are represented by the series connection of capacitors C_{ox} and C_{Si}, and substrate loss is included through the addition of resistor r_{Si} in parallel with C_{Si}, as in Fig. 3(b).

Circuit realizations for the ideal transformer subcircuit of Fig. 4 are shown in Fig. 5. Synthesis of a model directly from the circuit equations for magnetic coupling between current loops results in the direct-form model shown in Fig. 5(a). Inductances L_P and L_S model the self-inductances of the primary and secondary windings, respectively. Mutual coupling between windings is modeled by the dependent current sources, which are weighted by parameters M_{12} and M_{21} (note that $M_{12} = M_{21}$ for a passive, reciprocal transformer).

Thévenizing the dependent current source on the secondary side of the direct-form model gives the dual-source model shown in Fig. 5(b). In this equivalent circuit, the transformer turns ratio n is an explicit parameter. Current flowing through magnetizing inductance $k_m L_P$ gives rise to voltage v_P which

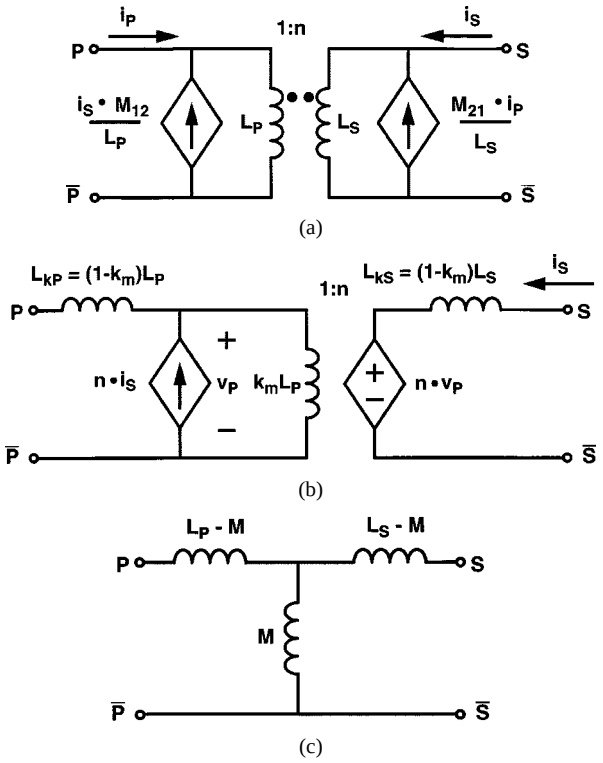

Fig. 5. CAD models for magnetic coupling in a $1:n$ transformer. (a) Direct form model. (b) Dual-source model. (c) T-section model.

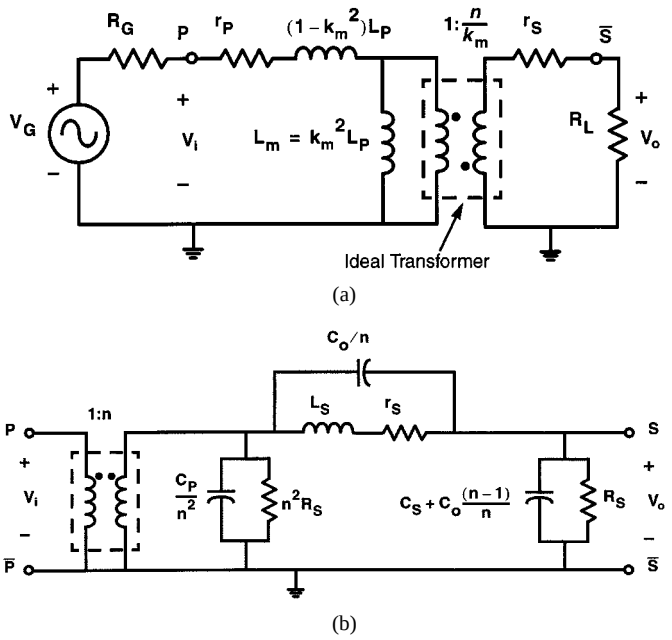

Fig. 6. Transformer equivalent circuits. (a) Low-frequency model with leakage shifted to primary. (b) High-frequency equivalent circuit with leakage shifted to secondary.

controls the dependent voltage source on the secondary side. Note that this results in an ideal $1:n$ transformation for voltage between the internal primary and secondary. The actual terminal voltage is modified by current flow through leakage inductances L_{kP} and L_{kS} placed in series with the primary and secondary windings. The model shown in Fig. 5(b) has the leakage inductance partitioned equally between windings, as the mutual inductance is

$$M^2 = (L_P - L_{kP})(L_S - L_{kS}). \tag{4}$$

This arbitrary assignment of leakage inductance is not unique [i.e., (4) cannot explicitly define two unknown leakage inductances] and other combinations are possible. For example, if all the leakage inductance is moved to the primary winding, then

$$L_{kP} = L_P(1 - k_m^2) \quad \text{and} \quad L_{kS} = 0. \tag{5}$$

This combination also gives the same terminal behavior as the assignment shown in Fig. 5(b).

The T-section model of Fig. 5(c) uses three inductors to model the mutual coupling between windings. This model simplifies hand analysis of circuits incorporating transformers, however, it is only valid for ac signals because there must be isolation of dc current flow between the primary and secondary loops in a physical transformer.

V. Frequency Response

It is useful to consider simplifications of the compact model to determine the circuit elements that have the greatest impact on the operational bandwidth of the transformer. This information is used to develop guidelines for monolithic transformer design and explain experimental observations in terms of equivalent circuit parameters. The series and shunt inductive elements define many characteristics of the frequency response, and a simplified equivalent circuit at low frequencies is shown in Fig. 6(a). The assignment of leakage inductance between primary and secondary is arbitrary, as described previously, and here the secondary leakage has been shifted to the primary in order to simplify the equivalent circuit.

It is clear from Fig. 6(a) that the shunt inductor in the primary affects the low end of the frequency response by shunting energy to ground, while the series element blocks transmission of the signal from primary to secondary as the operating frequency increases. The terms low, mid, and high frequency used in the following discussion are in the relative sense implied by the effects of these two elements.

A. Response at Low Frequency

The series combination of load resistance R_L and secondary winding loss r_S can be reflected to the primary side of the transformer as

$$R_r = \frac{(R_L + r_S)}{(n/k_m)^2}. \tag{6}$$

The reflected resistance R_r appears in parallel with the shunt magnetizing inductance L_m, shown in Fig. 6(a). The dc value of r_S ($r_{\rm dc}$) is determined by the unwound length of the winding ($l_{\rm winding}$) and the sheet resistivity of the metallization (r_{sh}) according to the equation

$$r_{\rm dc} = \frac{l_{\rm winding}}{w}\, r_{sh}. \tag{7}$$

For an integer number of turns, the unwound length of a square Frlan transformer (for example) with an integer number of turns N_t is given by

$$l_{\text{winding}} = 4N_t(\text{OD} - w) - 16(w+s)\frac{N_t(N_t-1)}{2} \qquad (8)$$

for $N_t \geq 2$. Similar expressions can be derived for the other winding configurations.

At the lower edge of the passband, the impedance of the magnetizing inductance (ωL_m) is small relative to R_r, and therefore little of the input signal v_i is transmitted to the load. As the operating frequency increases, the effect of the magnetizing inductance on the frequency response diminishes as its reactance becomes large relative to the reflected load and generator resistances. At relatively high frequencies, the leakage inductance in series with the generator impedance blocks signal transmission to the transformer output, and therefore attenuation of the transformer increases again.

Assuming that the reflected and effective generator resistances are approximately equal (i.e., $R_G + r_P = R_r$) and a $1:1$ turns ratio, it can be shown for the equivalent circuit of Fig. 6(a) that the fractional bandwidth of the magnetic path is

$$\frac{f_u}{f_l} = \frac{1+k_m}{1-k_m}, \qquad \text{for } k_m < 1 \qquad (9)$$

where fractional bandwidth is defined as the ratio of the upper and lower cut-off frequencies f_u/f_l. The relationship between bandwidth and k-factor, defined by (9), and the total attenuation from primary to secondary ports at the lower cut-off frequency f_l are plotted in Fig. 7. For a typical k-factor of 0.8, the monolithic transformer bandwidth is greater than three octaves ($f_u/f_l = 9$) with an attenuation ($|S_{21}| = 2v_o/v_G$) of 3.8 dB at the lower edge of the passband. As the k-factor approaches unity, the fractional bandwidth increases dramatically and the total attenuation at the lower cut-off frequency approaches the ideal ($|S_{21}| = -3$ dB, or $|v_o/v_i| = 1$), as shown in Fig. 7. Thus, a large k-factor is necessary to minimize attenuation and maximize the transformer bandwidth. Note that this analysis ignores the effects of ohmic loss in the windings and parasitic capacitances, which are substantial in monolithic transformers.

B. Mid-Band Response

As the operating frequency continues to increases, the attenuation through the transformer reaches a minimum in the passband. Losses in the passband are caused by dissipation of the windings and the conductive substrate for devices fabricated on silicon. In most cases, the series parasitics in the transformer compact model dominate the midband response, because the source and load impedances used in RF circuits are typically an order of magnitude lower than the shunt parasitics (on the order of tens of ohms for the source/load compared to hundreds of ohms for the shunt parasitics).

The simplified compact model of Fig. 6(a) can be used to predict the midband response if the capacitive parasitics are negligible. Assuming a $1:1$ transformer with a symmetrically loaded winding so that

$$R = R_G + r_P = R_L + r_S \qquad (10)$$

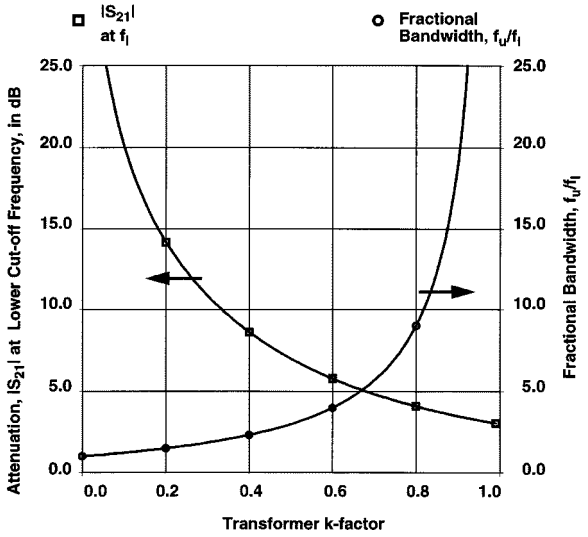

Fig. 7. Fractional bandwidth and attenuation versus transformer k-factor.

it can be shown that the maximum signal transmission in the passband is

$$|S_{21}| = \frac{2v_o}{v_G} = \frac{k_m(R_L)}{R} \qquad (11)$$

which occurs at a frequency

$$f_{pk} = \frac{R}{2\pi L_P\sqrt{1-k_m^2}}. \qquad (12)$$

These equations show that the signal attenuation in the passband can be estimated from the k-factor and termination resistances. As the k-factor decreases, both the signal transmission and the fractional bandwidth of the transformer are diminished, and the attenuation minimum shifts closer to the lower cut-off frequency of the transformer winding ($f_l = R/(2\pi L_P)$). Thus, a large k-factor is needed to reduce attenuation in the passband and maximize the usable bandwidth of the component.

C. High-Frequency Response

Parasitic capacitances are difficult to determine accurately (numerical analysis is normally required) and capacitive effects are best investigated from simulation of a particular case. However, some qualitative observations on the behavior of monolithic transformers can be made from the high-frequency equivalent circuit shown in Fig. 6(b). Here, a $1:n$ turns ratio transformer with $k_m = 1$ is assumed, and the significant high-frequency parasitics from the compact model of Fig. 4 have been shifted to the secondary loop. The shunt elements are represented by a R–C equivalents, as is valid at a given frequency, and the effect of the shunt inductance in the primary is again assumed negligible. The value of the interwinding capacitance is modified by the voltage transfer ratio n when moved from primary to secondary loops due the Miller effect. The sign of the transfer ratio can be either positive (noninverting) or negative (inverting configuration), which leads to different behavior at higher frequencies. For the noninverting connection, n is positive and the π-type L–C section in the transformer secondary has a bandpass response

with a transmission zero due to the effect of Co in parallel with L_S. This zero causes a notch in the high-frequency response. However, the inverting connection behaves differently at higher frequencies. The voltage transfer ratio n is negative in the inverting connection, which causes the bridging capacitor Co to have a positive reactance that *decreases* with increasing frequency. Thus, the magnitude response at high frequencies resembles a lowpass filter with a comparatively higher cut-off than for the noninverting connection, due to absence of the transmission zero.

The substrate and interwinding parasitic capacitances resonate with the inductance of each winding, and above this self-resonance, the reactance at the transformer input appears capacitive. Hence, the self-resonant frequency is often used as a figure of merit to define and compare the upper frequency limit for transformers.

D. Differential versus Single-Ended Drive

It has been demonstrated that differential drive of a microstrip winding gives a higher quality (Q)-factor and broader bandwidth than when a single-ended source is used [27]. Consider the equivalent circuit of the single microstrip line section, shown in Fig. 8. Here, a simplified equivalent circuit consisting of C_p and R_p represents the electrical behavior of C_{ox}, $C_{\rm Si}$, and $r_{\rm Si}$ at any given frequency.

For single-ended excitation, Port 2 is grounded and the equivalent circuit is connected as a one-port. The input impedance at Port 1, defined as Z_{se}, becomes a parallel combination of two components: Z_B, representing the inductance and series dissipation (L_s and r_s), and Z_A, representing the shunt $r_p - C_p$ parasitic elements, as illustrated in Fig. 8(a).

For a differential excitation, where the signal is applied between the two ports (Port 1 and Port 2), the input impedance Z_d is due to the parallel combination of $2Z_A$ and Z_B. Since the substrate parasitics are connected via the ground plane, the two shunt elements are now in series. The equivalent circuit is shown in Fig. 8(b).

Note that the impedance of the substrate parasitics in the equivalent circuit are $2r_P$ and $2C_P$ for the differential case, which are double the value for single-ended excitation (i.e., just r_P in parallel with C_P, single-ended). Therefore, at lower frequencies, the input impedance in either the shunt or the differential connections is approximately the same. However, as the frequency increases, these parasitics have a higher impedance at a given frequency when excited differentially than they do in the single-ended connection. This reduces the real part and increases the reactive component of the input impedance. Therefore, the Q-factor is improved when driven differentially, and moreover, a wider operating bandwidth is realized for no extra cost in processing.

E. Transformer Tuning

Capacitors placed in shunt with the primary and secondary windings tune a monolithic transformer and decrease the losses between input and output ports. As seen from the simplified compact 'T' model of Fig. 9, the shunt capacitance and leakage

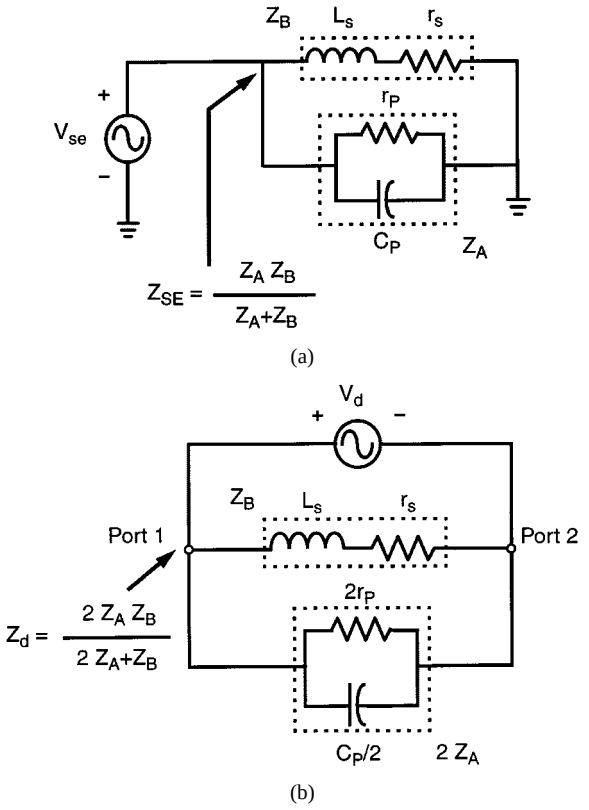

Fig. 8. Differential versus single-ended excitation. (a) Single-ended model. (b) Differential model.

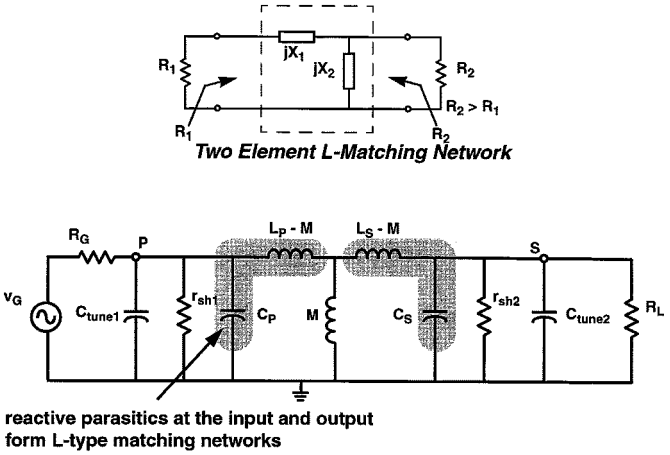

Fig. 9. Simplified transformer model illustrating resonant tuning at both ports.

inductance at each port form lossy L-section matching networks. The two element L-section will modify the impedance appearing across the terminals of the transformer to a lower impedance at the internal transformer nodes (in the compact model). By appropriate selection of the tuning capacitance at each port, the impedance appearing in shunt with the internal transformer can be represented as a shunt R–C equivalent. When the total shunt capacitive component C is parallel resonant with the magnetizing inductance L_m, the two ports are matched and transmission losses are minimized.

The attenuation caused by leakage in a low k-factor transformer is substantial, as shown in Fig. 7, however, the loss can be reduced by resonant tuning. Unfortunately, a larger portion

TABLE I
TECHNOLOLGY PARAMETERS [28]

Parameter	Value
Substrate resistivity	15 Ω-cm
Substrate thickness	200 μm
Silicon dielectric constant	11.7
Oxide thickness (M3-sub.)	5.75 μm
Oxide thickness (M3-M2)	1.9 μm
SiO_2 dielectric constant	3.9
Metal resistivity	0.03 Ω-μm
Top Metal (M3) thickness	2.07 μm
Second Metal (M2) thickness	0.9 μm

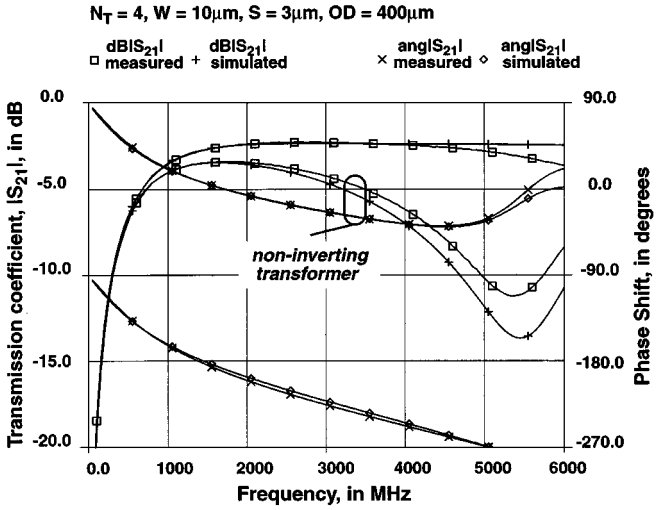

Fig. 10. Measurement versus simulation for 1 : 1 spiral transformers.

of the power entering the transformer is dissipated by ohmic losses in the windings themselves as the k-factor is reduced. This is an important consideration because the ohmic losses of the windings are relatively high due to the thin metallization used in fabrication. The effective load reflected from the secondary back to the primary is proportional to the square of the transformer k-factor, as seen from the low-frequency model of Fig. 6(a). Hence, as the k-factor drops, so does the load at the internal node as seen from the primary side. Therefore, a high k-factor is still desirable in order to limit losses in the passband when resonant tuning is used to reduce the attenuation.

VI. TRANSFORMER EXAMPLES

The performance of both spiral and symmetric transformers has been characterized in simulation and by fabricating and testing a number of different designs. The following square spiral layouts have been fabricated and tested: 1 : 1 inverting and noninverting, 1 : 3 and 1 : 5 inverting step-up designs, a 4 : 5 square symmetric balun, and a 2 : 1 : 1 symmetric trifilar transformer.

A. Inverting and Non-Inverting 1 : 1 Transformers

A 1 : 1 Frlan transformer consisting of four turns of 10-μm-wide top-level metal with a 3-μm conductor spacing and measuring 400 μm on each side (i.e., dimension OD in Fig. 2) has been fabricated and tested. The interwinding capacitance introduced by closely spaced conductors is acceptable in most applications. A summary of the important parameters of the fabrication process are listed in Table I [28]. A number of features of this technology are worth noting. The top-metal thickness is close to 2 μm, which is double the metal thickness available in most silicon VLSI technologies. Thicker metal reduces the ohmic losses in the primary and secondary windings of a planar transformer. Also, the 6-μm-thick insulating oxide layer reduces parasitic coupling to the semiconducting substrate, thereby improving the operating bandwidth and reducing in-band losses caused by shunt parasitic elements. Losses due to the substrate are further reduced through the use of a relatively high resistivity substrate (nominally 15 Ω-cm). Previous experience with both simulation and measurement of microstrip spiral inductors [9] has shown that the minimum conductor spacing improves the magnetic coupling between primary and secondary windings, and hence the closest line spacing ($s = 3$ μm) was chosen.

The frequency response (both magnitude and phase) of the square spiral (Frlan) transformer in both the inverting and noninverting connections is compared in Fig. 10. At low frequencies, the transmission of a signal from primary to secondary for a 50-Ω source and load (S_{21}) is low, because the input frequency is well below the self-inductance of the primary and secondary windings [note that S_{21} is, by definition, 6 dB larger than the voltage gain v_o/v_G, as defined in Fig. 6(a), with $R_G = R_L = 50$ Ω]. As the frequency increases, the coupling between input and output also improves, reaching a minimum in the operating band, which for this transformer is in the 1–3-GHz range. There is a substantial difference in the magnitude responses of the two connections, as seen from both the measured and simulated data shown in Fig. 10. This difference is mainly due to the effect of interwinding capacitance, which introduces a zero in the response of the noninverting transformer as previously outlined in Section V-C. The phase difference between inverting and noninverting configurations is 180 degrees at low frequencies, as expected, but deviates significantly above 3 GHz, which defines the upper edge of the transformer's operating band. The simulated and measured responses agree well in both phase and magnitude up to the first self-resonant frequency of the two windings, where the assumption of lumped behavior in the simulation model no longer applies. This occurs at approximately 5 GHz.

B. Comparison of Planar and Overlay Configurations

The winding configuration and technology used in fabrication are other important factors that determine the frequency response of a monolithic transformer. In order to investigate this, two 1 : 1 transformers were designed given the technology parameters listed in Table I. The first design is a four-turn Frlan transformer consisting of 10-μm-wide conductors spaced 3 μm apart, with an outer dimension (OD) of 400 μm, as in Section VI-A. The second design is a four-turn Finlay transformer. The conductor width and conductor spacing is identical for both designs, but the dimensions of the Finlay transformer

TABLE II
PARAMETERS FOR 1 : 1 PLANAR AND OVERLAY TRANSFORMERS ($w = 9\,\mu$m, $s = 3\,\mu$m)

Winding Configuration	OD, μm	L_P, nH	d.c. r_P, Ω	d.c. r_S, Ω	k_m	f_{SRF}, GHz	Minimum Attenuation, dB
Frlan inverting	400	8.5	8.3	8.3	0.84	4.9	2.25 @ 2.5GHz
Frlan non-inverting	400	8.5	8.3	8.3	0.84	5.2	3.22 @ 1.4GHz
Finlay inverting	309	8.5	5.7	12.7	0.90	2.5	2.84 @ 2.0GHz
Finlay non-inverting	309	8.6	5.7	12.7	0.90	6.1	3.50 @ 1.6GHz

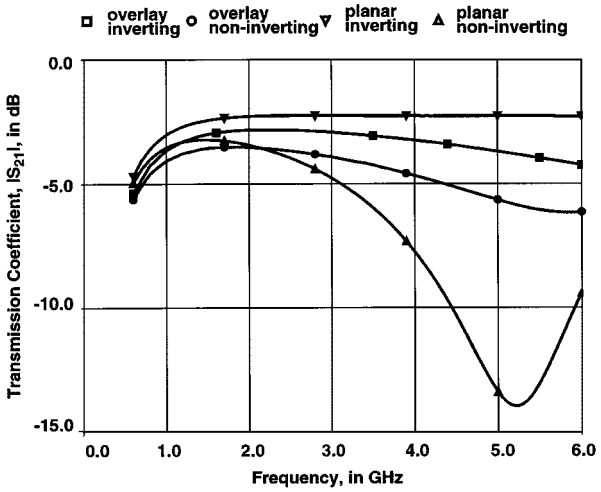

Fig. 11. Magnitude response for planar and overlay configurations.

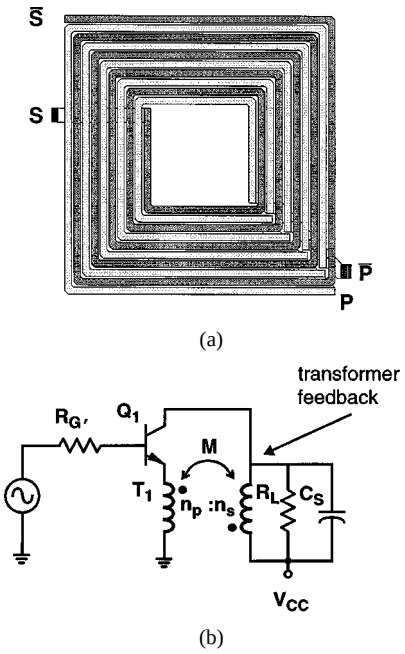

Fig. 12. 1 : 5 step-up transformer and application. (a) 1 : 5 step-up transformer layout. (b) Transformer coupled feedback amplifier.

are chosen to match the self-inductance of the Frlan design (OD = 309 μm). The simulated low frequency parameters of the transformer compact model (i.e., L_P, r_P, and r_S) are compared in Table II.

The data shows that the k-factor of the Finlay transformer is 7% higher than the Frlan design due to tighter coupling of the magnetic field in the overlay configuration. The main advantage of overlaying the windings is that approximately one-half of the chip area is required to realize the same self-inductance, and hence each winding for the Finlay transformer is shorter in its unwound length. This leads to a lower r_P for the Finlay transformer (5.7 Ω compared to 8.5 Ω), however, the resistance of secondary winding is higher (at 12.7 Ω) because thinner metal is used for the lower-level (i.e., secondary) winding. This is a limitation typical of current silicon VLSI technologies.

The magnitude response of each transformer is plotted in Fig. 11 for both inverting and noninverting connections. It can be seen from the figure that lower attenuation is achieved using the inverting connection, as predicted from high frequency analysis of the compact model. The pronounced dips in the magnitude response in the noninverting connection are caused by the effect of the interwinding capacitance (as described in Section V-C). The notch in the response is more pronounced for the planar (Frlan) transformer because the ohmic losses of the windings are lower, resulting in a higher Q-factor. Attenuation is highest for the overlay transformer connected in the noninverting configuration because the secondary winding has a relatively high series resistance. The minimum passband attenuation and the frequency where this occurs (listed in Table II) agree fairly well with the predictions from (11) and (12), which are 2.7 dB at 2 GHz for the Frlan and 2.6 dB at 2.5 GHz for the Finlay transformer.

C. 1 : n Square Spiral Transformers

Turns ratios other than 1 : 1 are also possible. For example, a 1 : 5 step-up ratio between primary and secondary can be realized by sectioning one winding (e.g., the primary) into five individual turns rather than one continuous winding. These five single-turn windings are then connected in parallel to form a 1 : 5 step-up ratio between primary and secondary of the transformer. The 1 : 5 step-up design shown in Fig. 12(a) consists of ten turns of 10-μm-wide topmetal with a 3-μm conductor spacing, and measures 400 μm on each side. The primary winding (five individual turns) are lightly shaded in the figure rather than one continuous winding.

The basic compact model parameters (refer to Fig. 4) for 1 : 1, 1 : 3, and 1 : 5 transformers are compared in Table III. The transformers were simulated using the GEMCAP2 program and measured data was obtained from samples fabricated in the technology of Table I. The k-factor decreases slightly as the turns ratio was varied, which is expected as the number of turns on the secondary winding differs for each design. The total inductance on the primary (L_P in Table III) scales approximately as

TABLE III
COMPACT MODEL PARAMETERS FOR PLANAR TRANSFORMERS

Design	L_P, nH	L_S, nH	k_m	Cp_{ox}, fF	rp_{Si}, Ω	Cs_{ox}, fF	rs_{Si}, Ω
1:1 measured	7.87	7.87	0.82	390	30	418	29
1:1 simulated	7.49	7.49	0.82	450	25	487	21
1:3 measured	0.64	5.76	0.76	437	21	262	58
1:3 simulated	0.61	5.49	0.77	501	12	330	33
1:5 measured	0.39	9.75	0.76	374	27	342	35
1:5 simulated	0.36	9.00	0.76	359	31	361	32

the square of the turns ratio. The self-inductance and associated parasitics at the secondary (L_S and Cs_{ox} in Table III) are determined by the length of the winding and increase with increasing winding length. The ratio of self-inductance to parasitic capacitance at the primary decreases dramatically for larger step-up ratios, and therefore the driving point impedance at Port 1 must be kept low in order to efficiently couple a signal into a step-up transformer primary.

The step-up transformer is an almost ideal feedback element for an RF amplifier, and can be used as a narrowband alternative to a broadband resistive network. The benefits of negative feedback in amplifier design are well known, however, a broadband feedback amplifier cannot meet the sub-3-dB noise figure required for many wireless applications. Feedback via mutual magnetic coupling in a $1:n$ transformer, as shown in Fig. 12(b), allows for control of amplifier gain and linearity without introducing excessive noise. Note that primary of transformer T_1 is driven from the emitter, which is a low impedance source, and the secondary of T_1 is made resonant using C_S to realize the desired amplifier load impedance. A low supply voltage is possible, since ohmic drops in the bias path are nearly eliminated. A 1-dB noise figure RF preamplifier with 12-dB gain and input third-order intercept point of -4 dBm that consumes 2 mW from a 1-V supply has been realized using transformer feedback [10], [2]. This level of performance was achieved with a production silicon IC process flow that was not optimized for RF performance from the passive components.

D. Multifilament Transformers and Transformer Baluns

The $1:1$ and $1:n$ transformers described in the previous sections of this paper consist of two independent windings (or conducting filaments) and are classified as bifilar transformers. Multifilament transformers can also be constructed on-chip. These devices are used to implement power dividers/combiners and baluns.

A balun is a device which couples a balanced circuit to an unbalanced one. There are many structures used to implement baluns at RF and microwave frequencies, although a differential amplifier is the most commonly used method for unbalanced-to-balanced signal conversion on-chip. Microwave balun structures such as the Lange, rat-race, and branch line coupler require physical dimensions on the order of the signal wavelength and so these devices consume too much chip area when operating below approximately 15 GHz [29]. The transformers shown in Fig. 2 can also implement a balun by grounding one of the windings at the electrical center, or center tap. The electrical and physical center of a winding differ for all of the spiral designs shown in Fig. 2, which is a disadvantage of asymmetric layouts.

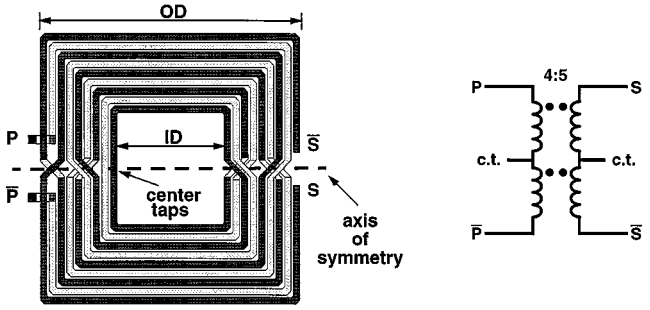

Fig. 13. Square symmetric (Rabjohn) balun.

A square symmetric layout, first proposed by Rabjohn [8] and illustrated in Fig. 13, solves this problem. This transformer consists of two groups of interwound microstrip lines that are divided along a line of symmetry running horizontally, as shown in Fig. 13. The groups of lines are interconnected in a way which brings all four terminals to the outside edge of the transformer layout, which is an advantage when connecting the transformer terminals to other circuitry. Also, the midpoint between the terminals on each winding, or the center tap, can be located precisely in the symmetric layout as indicated in Fig. 13. The turns ratio for the example shown is $4:5$ between primary and secondary.

The measured and simulated responses for this balun are compared in Fig. 14. The experimental transformer is designed with OD $= 325$ μm, 8-μm linewidth, 3-μm line spacing, and fabricated with the technology described in Table I. The slight difference in magnitude response at the inverting and noninverting secondary ports is clearly seen from the measurements. This is due to the effect of interwinding capacitance (as described in Section V-C). The effect is not reduced by adding tuning capacitance in shunt with the transformer ports. Capacitors connected at the input and output ports (425 fF across the primary and 1.7 pF across each secondary winding) tune the balun to match the (50-Ω) source to the secondary load, and the tuned response is also plotted on Fig. 14. The measured transmission loss is reduced from over 5 dB to very close to the ideal (3 dB) by tuning. The phase error between secondary ports of the tuned balun is also shown on Fig. 14,

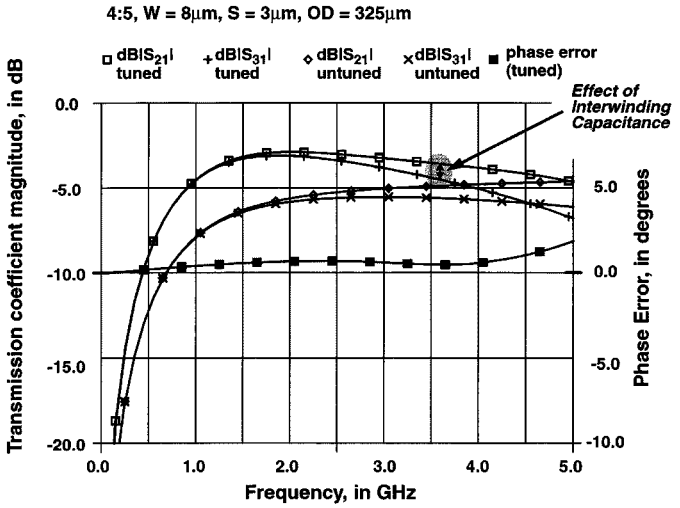

Fig. 14. Frequency response of a monolithic transformer balun.

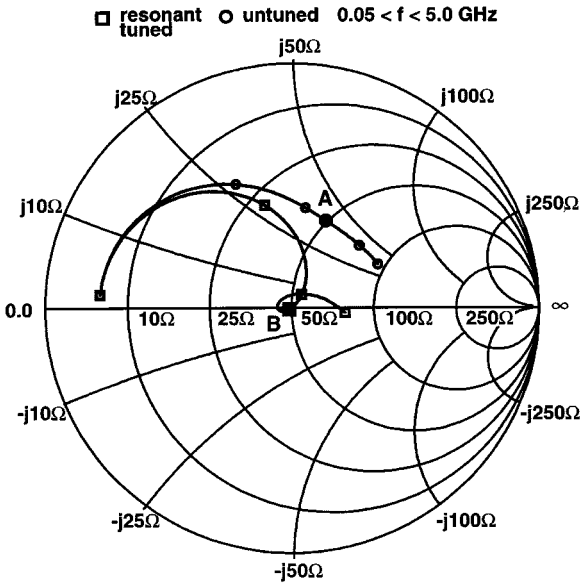

Fig. 15. Input impedance of the 4 : 5 balun.

where the phase error is the deviation from a 180 phase difference between ports. This error is on the order of 1 degree in the desired passband for the balun (2000–3000 MHz).

The measured input impedance for the 4 : 5 step-up balun was determined and plotted on the complex impedance chart shown in Fig. 15 for a frequency range from 10 MHz to 5 GHz. The secondary load resistance is matched to the real part of the transformer output impedance R_{LS} which includes losses in the windings. This resistance for a given transformer turns ratio n, generator resistance R_G, and ohmic losses of the primary and secondary windings r_P and r_S, is given by

$$R_{LS} \approx \frac{n^2}{2}(R_G + r_P) + r_S. \tag{13}$$

Here, $n = 1.25$, $R_G = 50\ \Omega$, $r_P = 8.5\ \Omega$, and $r_S = 10.2\ \Omega$.

Point A on the impedance plot is the untuned input impedance at 2.4 GHz, $47 + j40\ \Omega$. The addition of the tuning capacitors (425 fF and 1.7 pF at the primary and secondary terminals, respectively) establishes a resonance with primary and secondary

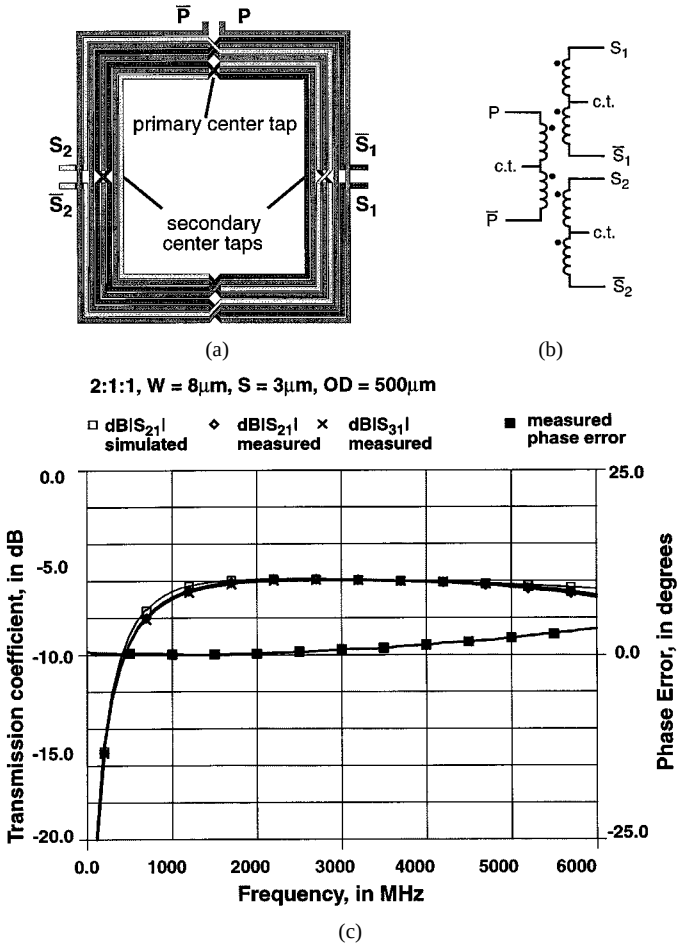

Fig. 16. Trifilar balun. (a) Square symmetric trifilar balun layout. (b) Functional equivalent circuit. (c) Frequency response.

windings so that the input impedance is 50 Ω at approximately 2.4 GHz (point B on Fig. 15). It should be noted that the leakage inductance at each port is fixed by the transformer design, and therefore the range of impedances which can be realized by resonant tuning with shunt capacitors is limited. In conventional two-element L–C matching, a wider range of impedances can be matched since both "L" and "C" are variable. However, tuning capacitors can also be placed in series with each port to extend this range.

The physical layout of a square symmetric *trifilar* balun measuring 500 μm on a side is shown in Fig. 16(a), and the schematic is illustrated in Fig. 16(b). The transformer consists of three groups of interwound 8-μm-wide microstrip lines with a 3-μm line spacing, which are divided along a line of symmetry running vertically and horizontally through the center. The four groups of lines are connected so that all terminals are brought to the outside edge of the layout, which is advantageous when using the transformer with other circuitry. The three separate windings of the balun (i.e., one primary and two secondary windings) are indicated by shading of the conductors.

The measured performance of the trifilar balun when driven differentially is illustrated in Fig. 16(c). The forward transmission of power from the primary input P to secondary outputs $\overline{S1}$ (S_{21} in Fig. 16) and $\overline{S2}$ (S_{31}) of the balun is plotted against the left axis of the figure. The other terminals of the balun were

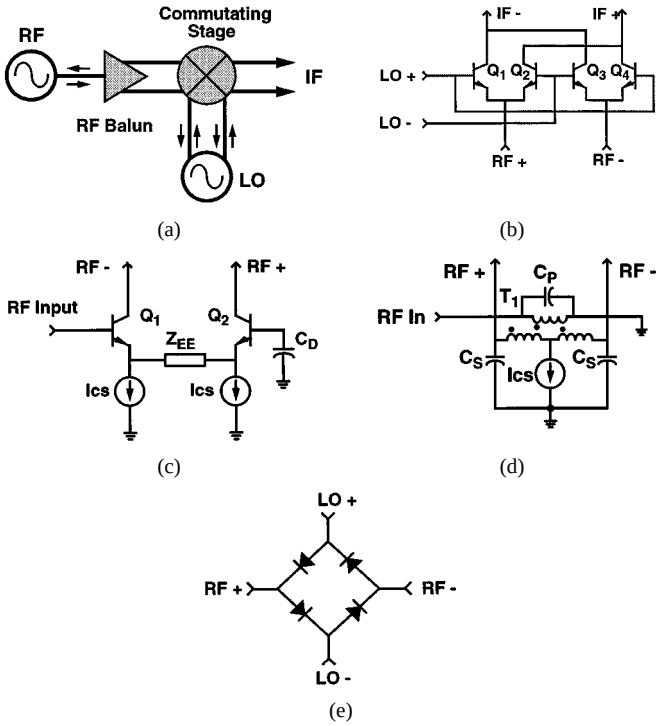

Fig. 17. Mixer circuits. (a) Balanced mixer block diagram. (b) BJT commutating stage. (c) Differential pair balun. (d) RF transformer balun. (e) Diode commutator.

grounded for this measurement. Again, excellent agreement is seen between the predictions of the computer model and the de-embedded measurements from RF on-wafer probing. The phase error between secondary windings of the balun is also shown. Note that very low phase and amplitude error is seen in the desired passband from 1–4 GHz due to the use of a fully symmetric layout and differential drive.

E. Transformer Baluns in Mixers

Interstage coupling using on-chip magnetic elements is an alternative technique of aggressively improving a mixer's performance, which has a different set of design trade-offs from the better-known *RC* mixer topologies. The monolithic transformer balun can be used to improve the dynamic range of monolithic mixers [2].

A conventional IC doubly balanced demodulator, which is based on the Gilbert multiplier topology [30], can be viewed as a linear preamplifier stage followed by a differential down-converting mixer, as illustrated in Fig. 17(a). The input stage converts a single-ended RF input signal into a differential signal that drives the RF inputs of a four-transistor mixing quad [see Fig. 17(b)]. This is analogous to the function of a balun in RF and microwave mixer circuits and a differential amplifier is normally used for this purpose on an RF ICs [shown in Fig. 17(c)].

Gain in the input stage can be used to suppress noise introduced by the mixing quad, but this gain also reduces the upper limit on the mixer's dynamic range. However, distortion in the receive mixer usually defines the input intercept point for the receive chain in a modern transceiver. Hence, a Gilbert mixer is normally designed with little gain in order to maximize the linear range at the mixer's RF input.

With a passive transformer balun [as in Fig. 17(d)], the RF input can be matched to the mixing quad through the appropriate choice of transformer turns ratio. The passive balun introduces virtually no distortion to the RF signal, thereby preserving linearity. Resonant tuning must be used to ensure that the signal-to-noise ratio is not excessively degraded in the transformation. The transformer-coupled bipolar junction transistor (BJT) mixer has demonstrated a low noise figure (9.5 dB single-sideband (SSB) 50 Ω), and a relatively high third-order intercept point ($+6$ dBm) given that the circuit has conversion gain (7 dB) and operates from a 1.0-V supply [10].

Mixers with high linearity and 6–7-dB noise figures can be implemented on-chip using balun-coupled diode ring topologies. Input intercept points on the order of $+10$ dBm, or more, are possible for such mixers based on a quad of Schottky diodes, as in Fig. 17(e). The local oscillator (LO) power required to drive the diode mixer is a disadvantage when 50 Ω interfaces are used. However, in a completely monolithic implementation, the port impedances can be defined on-chip in order to reduce power consumption.

A mixer design utilizing monolithic trifilar baluns at the RF and LO inputs and a Schottky diode ring has also been developed for lower-power/low-voltage applications [14]. The design is derived from existing mixer architectures, such as the Gilbert multiplier and the doubly balanced diode ring mixer. From experimental measurements for an RF input of 5.3 GHz, LO at 5.55 GHz and IF at 250 MHz, the mixer attains -6.5 dB gain, 6.1-dB noise figure, and a $+8.2$-dBm IIP3. Although there is a conversion loss, the emphasis in this design is on linearity and improved dynamic range rather than conversion gain.

The transformer-coupled approach has the potential to realize a variety of proven mixer topologies, including image-reject designs [15], [31]. When implemented monolithically, these components can offer a significant advance in transceiver performance and integration level compared to the current state-of-the-art.

VII. Transformer Design

The goal of a design procedure for monolithic transformers is to attain the desired bandwidth with the lowest possible losses, while consuming as little chip area as possible. In this section, a procedure for estimating the initial size of a monolithic transformer will be given. Because of the complexities involved in the modeling and analysis of these components, any design procedure should involve simulation of the structure in order to confirm that the original performance requirements are satisfied.

The important figures of merit for the monolithic transformer are: k-factor (k_m), source and load impedance levels [R, from (10)], self-inductances of the individual windings, and the self-resonant frequency (which is determined by parasitic capacitances).

As seen from Fig. 7, a k-factor close to one gives the widest bandwidth. For narrowband applications such as cellular telephony, little useful selectivity is possible because the Q-factor of a monolithic transformer's windings is on the order of 5 or less. Thus, the transformer bandwidth will not affect the in-band response, even when resonant tuned.

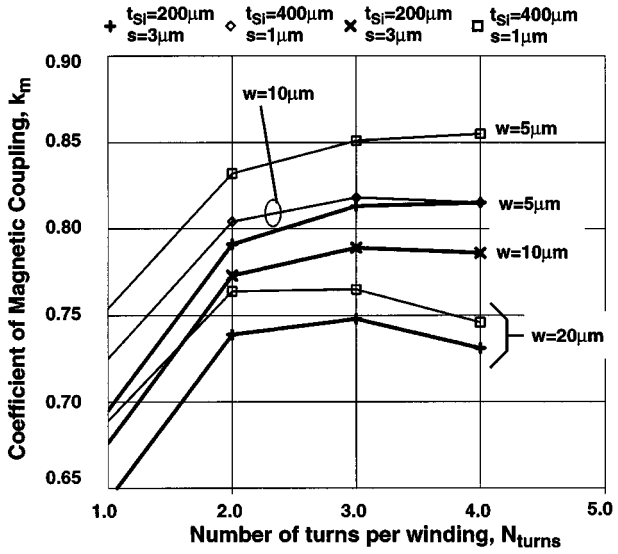

Fig. 18. k-factor versus number of turns for a 1 : 1 Frlan transformer with $L_{\rm self} = 5$ nH.

For a resonant *RLC* circuit, the −3-dB bandwidth (in Hertz) is given by

$$BW = 1/(2\pi R_{\rm eff} C_{\rm eff}) \tag{14}$$

where $R_{\rm eff}$ is the total resistance (including loading of the source) and $C_{\rm eff}$ is the total capacitance shunting the circuit. If a large self-inductance is used (e.g., 10 nH), a relatively small $C_{\rm eff}$ is needed to tune the transformer. A small self-inductance (e.g., 2 nH) requires more tuning capacitance, and (14) predicts a narrower bandwidth for a given load, $R_{\rm eff}$. Therefore, the selection of winding inductance influences the bandwidth when resonant tuning is applied. For relatively low terminal impedances (on the order of the conductor ohmic losses), the series parasitics (r_s and L_s in the transformer model) dominate the response and so wider conductors lines with relatively large parasitic capacitances may be used. When terminal impedances on the order of hundreds of ohms are used, shunt parasitics play a more important role in the overall response and therefore narrower conductor widths should be used.

A. Transformer k-factor

The relationship between k-factor and the parameters that influence the magnetic coupling between windings of a transformer fabricated on an IC is complex and it is best investigated using simulation tools.

To maximize magnetic coupling between windings (and hence k-factor), adjacent conductors should belong to different windings. The mutual magnetic coupling between adjacent conductors that belong to the same winding contributes self-inductance but not mutual inductance to the transformer and lowers the coupling coefficient.

The plot shown in Fig. 18 illustrates the variation in k-factor with the number of turns for a 1 : 1 turns ratio square spiral Frlan transformer [layout as in Fig. 2(b)]. The curves plotted on the figure were generated using the Greenhouse algorithm [17] for transformer layouts having a constant self-inductance of 5 nH. Two sets of fabrication parameters were chosen: a line spacing and winding metal thickness of 1 μm on a 400-μm-thick substrate (similar to many VLSI processes), and the parameters for the 1 : 1 transformers that were fabricated and described previously (see Table I). The effect of metal width (and spacing) on the magnetic coupling is clearly apparent from the figure. For a given number of turns, the lines of magnetic flux which couple between windings increases as the metal width decreases. There is a large improvement in k-factor as the number of turns is increased from one to two, because of coupling between adjacent lines. The number of metal lines running in parallel increases with the number of turns, and because the magnetic coupling decreases quickly with the separation between parallel conductors, the k-factor quickly tends to a limiting value for a given metal width. The data shown in the figure indicates that a design with three to four turns is optimum.

B. Design Procedure

As a first step, the inductance required for each winding must be determined from consideration of the terminal impedances and center frequency specification. For example, (12) can be used to compute the winding self-inductance (of a 1 : 1 transformer) for a given center frequency f_{pk} and loading R. In a narrowband system, the inductance of the transformer winding can often be made resonant with a parasitic capacitance, and so the capacitance of the source and/or load must be considered in the process of determining the winding self-inductance and turns ratio. Additional capacitance may be added in shunt at the ports of the transformer to tune the device to a given frequency and reduce the transmission losses. Resonant tuning reduces the bandwidth of the transformer [as per (14)] and hence selection of center frequency, bandwidth, and winding inductance are closely related. For applications where bandwidth is a consideration, the inverting connection should be used.

It was shown previously (Fig. 18) that the transformer k-factor improves as the width of the winding decreases, and therefore the smallest practical linewidth should be used in the design. However, the high ohmic losses in the windings of a monolithic transformer must also be considered. These losses modify the impedances seen at each port when the transformer is impedance matched to the source and load, and also contribute noise in the final circuit. Narrowly spaced conductors improve the magnetic and electric coupling between windings. In most cases, line spacing s close to the minimum allowable for the technology results in the best overall performance (i.e., additional interwinding capacitance is less important that the improvement in k-factor).

Knowing the winding inductance, number of turns, and conductor width and spacing, the physical dimensions of a transformer can be estimated with a design aid such as the one shown in Fig. 19. This graph (also generated from Greenhouses' algorithm) illustrates the inductance per unit of length of a given winding as a function of the OD for a four-turn 1 : 1 Frlan transformer. Points on the curves shown in the figure are all physically realizable.

As an example, assume that a center frequency of 2 GHz in a 50-Ω system is required. Equation (12) predicts a winding

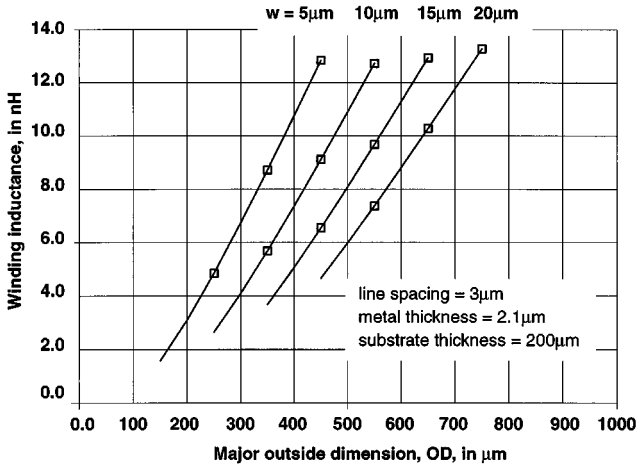

Fig. 19. Design curves for a four-turn spiral transformer.

inductance of approximately 7 nH assuming a typical k_m of 0.8. From Fig. 18, this k-factor is achievable for a conductor width of 10 μm if a four-turn layout is used. The design chart of Fig. 19 is then used to determine that an OD of approximately 400 μm is needed. The unwound length l_{winding} is 5 mm [from (8)] and the total winding resistance is 7.5 Ω for a metal sheet resistivity of 0.15 Ω/sq. This winding resistance could be included in the termination resistance [R in (12)] and the design values further refined by iteration.

VIII. Conclusion

The characteristics of various types and configurations of monolithic microstrip transformers have been presented from both simulation and measurement of devices fabricated in an advanced silicon VLSI technology. Performance degradation due to transformer parasitics were identified and the use of resonant tuning to reduce transmission losses described. A simplified design procedure for determining the layout dimensions of a transformer based on electrical specifications was also outlined. The advantages offered by monolithic transformers for RF IC design were illustrated using typical applications examples.

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References

[1] J. R. Long and M. A. Copeland, "Modeling of monolithic inductors and transformers for silicon RFIC design," in *Proc. IEEE MTT-S Int. Symp. Technologies for Wireless Applications*, Vancouver, BC, Canada, Feb. 1995, pp. 129–134.

[2] J. R. Long and M. A. Copeland, "A 1.9 GHz low-voltage silicon bipolar receiver front-end for wireless personal communication systems," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1438–1448, Dec. 1995.

[3] K. Shibata, K. Hatori, Y. Tokumitsu, and H. Komizo, "Microstrip spiral directional coupler," *IEEE Trans. Microwave Theory Tech.*, vol. 29, pp. 680–689, July 1981.

[4] S. A. Jamison, A. Podell, M. Helix, P. Ng, and C. Chao, "Inductively coupled push–pull amplifiers for low cost monolithic microwave ICs," in *Proc. IEEE GaAs IC Symp.*, Oct. 1982, pp. 91–93.

[5] D. Ferguson, P. Bauhahn, J. Keuper, R. Lokken, J. Culp, C. Chao, and A. Podell, "Transformer coupled high-density circuit technique for MMIC," in *Proc. Monolithic Microwave IC Symp.*, May 1984, pp. 34–36.

[6] E. Frlan, S. Meszaros, M. Cuhaci, and J. Wight, "Computer-aided design of square spiral transformers and inductors," in *Proc. IEEE MTT-S*, June 1989, pp. 661–664.

[7] A. Boulouard and M. Le Rouzic, "Analysis of rectangular spiral transformers for MMIC applications," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1257–1260, Aug. 1989.

[8] G. G. Rabjohn, "Monolithic microwave transformers," M.Eng. thesis, Carleton University, Ottawa, ON, Canada, Apr. 1991.

[9] J. R. Long and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for Silicon RF ICs," *IEEE J. Solid-State Circuits*, vol. 32, pp. 357–369, March 1997.

[10] J. R. Long, M. A. Copeland, S. J. Kovacic, D. S. Mahli, and D. L. Harame, "RF analog and digital circuits in SiGe technology," in *Proc. ISSCC*, Feb. 1996, pp. 82–83.

[11] J. J. Zhou and D. J. Allstot, "Monolithic transformers and their application in a differential CMOS RF low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2020–2027, Dec. 1998.

[12] B. Jansen, K. Negus, and D. Lee, "Silicon bipolar VCO family for 1.1 to 2.2 GHz with full-integrated tank and tuning circuits," in *Proc. ISSCC*, Feb. 1997, pp. 392–393.

[13] M. Zannoth, B. Kolb, J. Fenk, and R. Weigel, "A fully integrated VCO at 2 GHz," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1987–1991, Oct. 1998.

[14] D. T. S. Cheung, J. R. Long, R. Hadaway, and D. Harame, "Monolithic transformers for Silicon RF IC design," in *IEEE Bipolar and BiCMOS Technology Meeting*, Sept. 1998, pp. 105–108.

[15] J. R. Long and M. Maliepaard, "A 1-V 900-MHz image-reject downconverter in 0.5-μm CMOS," in *Proc. CICC*, May 1999, pp. 665–668.

[16] W. Simbuerger, H.-D. Wohlmuth, and P. Weger, "A monolithic 3.7-W Silicon power amplifier with 59% PAE at 0.9 GHz," in *Proc. ISSCC*, Feb. 1999, pp. 230–231.

[17] H. M. Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE Trans. Parts, Hybrids and Packaging*, vol. PHP-10, no. 2, pp. 101–109, June 1974.

[18] J. N. Burghartz, D. C. Edelstein, M. Souyer, H. A. Ainspan, and K. A. Jenkins, "RF circuit aspects of spiral inductors on Silicon," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2028–2034, Dec. 1998.

[19] J. N. Burghartz, D. C. Edelstein, M. Souyer, H. A. Ainspan, and K. A. Jenkins, "Multilevel spiral inductors using VLSI interconnect technology," *IEEE Electron Device Lett.*, vol. 17, pp. 428–430, Sept. 1996.

[20] J. M. Lopez-Villegas, J. Samitier, C. Cane, and P. Losantos, "Improvement of the quality factor of RF integrated inductors by layout optimization," in *Proc. Int. Microwave Symp.*, June 1998, pp. 169–172.

[21] H. J. Finlay, "U.K. patent application," 8 800 115, 1985.

[22] M. W. Geen, G. J. Green, R. G. Arnold, J. A. Jenkins, and R. H. Jansen, "Miniature multilayer spiral inductors for GaAs MMICs," in *Proc. GaAs IC Symp.*, Oct. 1989, pp. 303–306.

[23] S. S. Mohan, C. P. Yue, M. del Mar Hershenson, S. S. Wong, and T. H. Lee, "Modeling and characterization of on-chip transformers," in *Proc. IEDM*, Dec. 1998, pp. 531–534.

[24] D. Feucht, *Handbook of Analog Circuit Design*. San Diego, CA: Academic, 1990, ch. 8.

[25] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1470–1481, Oct. 1998.

[26] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstriplines on Si–SiO^2 system," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 869–881, Nov. 1971.

[27] M. Danesh, J. R. Long, R. Hadaway, and D. Harame, "A Q-factor enhancement technique for MMIC inductors in Silicon technology," in *Proc. Int. Microwave Symp.*, June 1998, pp. 217–220.

[28] D. C. Ahlgren *et al.*, "A SiGe HBT BiCMOS technology for mixed-signal applications," in *Proc. IEEE Bipolar and BiCMOS Technology Meeting*, Sept. 1997, pp. 195–197.

[29] R. Mongia, I. Bahl, and P. Bhartia, *RF and Microwave Coupled-Line Circuits*. Boston, MA: Artech House, 1999, ch. 8.

[30] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 365–373, Dec. 1968.

[31] J. R. Long, R. Hadaway, and D. Harame, "A 5.1–5.8GHz low-power image-reject downconverter in SiGe technology," in *Proc. IEEE Bipolar and BiCMOS Technology Meeting*, Sept. 1999, pp. 67–70.

John R. Long (M'95) received the B.Sc. degree in electrical engineering from the University of Calgary, Calgary, AB, Canada, in 1984, and the M.Eng. and Ph.D. degrees in electronics engineering from Carleton University, Ottawa, ON, Canada, in 1992 and 1996, respectively.

He was employed for 10 years by Bell-Northern Research Ltd., Ottawa (now Nortel Networks), involved in the design of GaAs ASICs for Gbit/s fiber-optic transmission systems. In 1996 he joined the faculty at the University of Toronto, Toronto, ON, Canada. His current research interests include low-power transceiver circuitry for highly integrated radio applications and electronics design for high-speed data communications systems.

Dr. Long was the recipient of the 1997 NSERC Doctoral Prize and the Douglas R. Colton and Governor General's Medals for research excellence. He is a Member of the Program Committee for the International Solid-State Circuits Conference (ISSCC) and Chair of the RF Program Committee for the IEEE Bipolar/BiCMOS Circuits and Technology Conference (BCTM).